## Purpose

This document outlines the tasks that Team AND has completed thus far, details the design decisions for our project, and finalizes which arbitrary function we will implement.

## Progress

### Completed Tasks:

* Developed schematics for the AND, OR, PASS A and 8:1 MUX components
* Simulated the functionality of the AND, OR, PASS A and 8:1 MUX components
* Developed schematics for the ADD, SUB, SHIFT and REGISTER components
* Simulated the functionality of the ADD, SUB, SHIFT and REGISTER components
* Decided to implement a Divider as our arbitrary function
* Wired the ALU in Cadence on the transistor level

### To Be Completed Prior to Final Presentation:

* Implement our Arbitrary Function
* Create a transistor level hierarchical schematic of the ALU
* Optimize and test our design to achieve minimum total area and power consumption

## Design Decisions and Optimizations

Our team made several significant design decisions that work toward creating the most efficient circuit possible. Most significantly, we made the decision to use pass gates to implement our shifter. Not only does this minimize the total area of the Shifter by reducing the number of transistors used, it also increases the speed at which the shift is accomplished by directly hardwiring the inputs to the desired outputs. This will be beneficial if we decide to use the shifter to implement our arbitrary function. The optimizations experienced in the shifter will propagate to our arbitrary function leaving us with a streamlined ALU operation.

Another optimization was made to the Subractor. We inverted the B input, set the carry-in bit to one and performed two’s compliment “subtraction.” This is extremely efficient because we eliminated the need to construct a separate subtraction block by reusing our adder. This will reduce the total area of the ALU significantly which, in turn, will diminish the total delay of an operation.

We also decided to design a Mirror Adder to execute the ADD function. This is a smart design decision because the Mirror Adder uses shorter transistor stacks and reduces the size of the Cin Transistors which creates a smaller load on the Cin path. The Mirror adder reduces the time it takes to do a computation while also decreasing the computation’s dependence on the Cout/Cin value.

Our team is on schedule to not only complete the project by the desired deadline, but to deliver a product that is efficient, fast and usable.